SNM Analysis of HEMT Based Highly Stable SRAM Cell

Balwant Raj¹, Parveen Kumar², Ernesto Limiti³, Sanjeev K. Sharma⁴ and Balwinder Raj⁵

¹UIET, Panjab University SSG Regional Centre, Hoshiarpur, 146021, India ^{2,4}Dr. B. R. Ambedkar National Institute of Technology, Jalandhar, 144011, India ³Full Processor, Department of Electronics Engineering, University of Rome, Italy ⁵National Institute of Technical Teachers Training and Research, Chandigarh, 160019, India

Abstract

This paper presents the analysis of Static Noise Margin (SNM) of HEMT based SRAM cell design for three deferent frequencies. The results obtained through our proposed design are compared and contrasted with reported data for the validation of our design approach. The Static Noise Margin (SNM) of HEMT based SARM cell was 355mV, 310mV and 245mV for frequency 5GHz, 20GHZ and 50GHZ respectively. The design and analysis of HEMT SRAM cell was done using TCAD tool. The high SNM is achieved for low frequency, which increases the stability of the proposed design.

Keywords

SRAM, SNM, HEMT, TCAD Tool, Stability

1. Introduction

The High Electron Mobility Transistor (HEMT) has a capacity to build up the prerequisites for High Momentum and Low Power ICs due to its High remove recurrence and high trans-conductance and diminished short channel impacts [1]. There are two fundamental kinds of semiconductor recollections for example SRAM and DRAM. Standard 6T SRAM cell gives quick admittance to information however it is actually enormous. It is utilized for little stockpiling and for quick store memory. On opposite side modern standard 1T1C DRAM cell is more modest than SRAM yet its speed is slow. Measure commonly utilized for principle memory [2-5]. From the assortment of advances which might be applied to start of semiconductor recollections, inside that the CMOS innovation has arisen as the prevailing innovation in manufacture of recollections like centralized computer, reserve, cushion, scratch-cushion, iphone, supercomputer, extra room of shopper hardware, and so forth, however GaAs innovation based memory configuration became famous because of its high velocity, low force scattering and capacity to work at high frequencies [5]. The requirement for rapid recollections has lead to the improvement of Gallium-Arsenide (GaAs) Random-Access Memories (RAMs). In this administrative work have been done for high solidness HEMT based SRAM Cell design.

2. Proposed HEMT SRAM Cell Design

Density, power consumption, and read and write access time are all typical design requirements for SRAM.To reduce circuit access time, pull up and pull down delays, just a single supply voltage should be used.In the proposed HEMT SRAM cell configuration, some essential features are taken into account.Figure 1 illustrates a schematic of the proposed high-speed HEMT-based SRAM cell.The SRAM cell is made up of four n-HEM and two p-HEMT transistors. Figure 1 shows how the source–

©2021 Copyright for this paper by its authors.

Use permitted under Creative Commons License Attribution 4.0 International (CC BY 4.0).

International Conference on Emerging Technologies: AI, IoT, and CPS for Science & Technology Applications, September 06–07, 2021, NITTTR Chandigarh, India

EMAIL: b.raj255@gmail.com (A. 1); parveen.eng@gmail.com (A. 2); limiti@ing.uniroma2.it (A. 3); sanjeev.nitj14@gmail.com (A. 4); balwinderraj@gmail.com (A. 5)

ORCID:0000-0001-5596-7209 (A. 1);0000-0001-7392-8844 (A. 2);0000-0003-4668-7461 (A. 3);0000-0002-4507-165X (A. 4); 0000-0002-3065-6313(A. 5)

Workshop BENNESSANT CEUR Workshop Proceedings (CEUR-WS.org)

gate back biasing in p-HEMTs, M1 and M2, is employed as a subthreshold current reduction circuit to minimize the cell's power dissipation. The cross-coupled M3 and M4 latch creates a healthy storage element with low static power dissipation. One write-only port is implemented by transistor M5, while a read-only port is implemented by transistor M6.

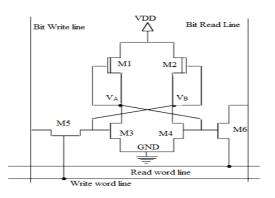


Figure 1: Proposed HEMT based SRAM cell

3. Result and Simulation

The results of the Static Random Access Memory (SRAM) cell designed with HEMT model are compared with reported results in the literature for the validation purpose as shown in Figure 2. We evaluated the reading and writing Static Noise Margin (SNM). The simulations of SRAM cell have been done using TCAD tool.

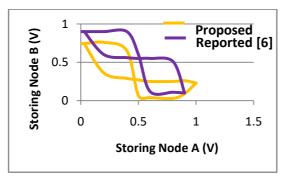


Figure 2:SNM Coparison with proposed and reported paper [6]

The simulation results of SRAM cell with various frequencies for both read and write operations have been carried out as shown in Figure 3. Significant increase in the SNM of proposed HEMT based SRAM cell design indicates improvement in the results obtained.

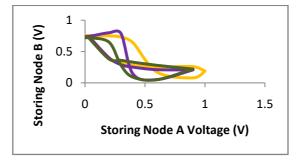


Figure 3:RSNM of HEMT SRAM cell with 5GHZ, 20 GHZ and 50 GHZ frequencies

 Table 1

 SNM Calculation of HEMT SRAM cell

Parameter	f = 5GHZ	f = 20GHZ	f = 50GHZ	Reported data
StaticNoiseMargin (mV)	355mV	310	245	238 [6]
Read SNM (mV)	305mv	281	208	194 [1]
Write SNM (mV)	416mv	378	267	200 [1]

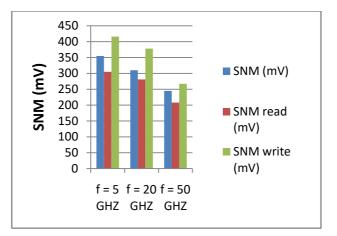


Figure 4: SNM, RSNM and WSNM vs. frequencies

The HEMT is high frequency transistor and at the higher frequencies HEMT based SRAM cell shows great Static Noise Margin (SNM), RSNM and WSNM is as shown in Figure 4. For frequency f = 5 GHZ the value of write SNM is shows best results while at frequency f = 20 GHZ SNM is slightly less than with compared to f = 5 GHZ.

4. Conclusion

In this work design and analysis of Static Random Access Memory (SRAM) cell have been carried out for evaluation of SNM. The simulation results have shown that our proposed HEMET based SRAM cell has been achieved significant increase in SNM over conventional SRAM cell, which validate our design approach. We compared and construct results of our proposed cell with previous reported data. The Static Noise Margin (SNM), Read Static Noise margin (RSNM) and Write Static Noise Margin (WSNM) shows excellent results over reported data.

5. References

- 1. A. Bernel, R. P. Ribas and A. Guyot, "GaAs MESFET SRAM using a new high memory cell", 5th european Gallium arsenide and related III-V compounds application symposium Bologna, Italy, september 3rd to 5th 1997.
- 2. CMOS Memory Circuits by Tegze P. Haraszti.
- B. Raj, A. K. Saxena and S. Dasgupta, "Analytical Modeling for the Estimation of Leakage Current and Subthreshold Swing Factor of Nanoscale Double Gate FinFET Device" Microelectronics International, UK, vol. 26, pp. 53-63, 2009.
- 4. B. Raj, A. K. Saxena and S. Dasgupta, "Nanoscale FinFET Based SRAM Cell Design: Analysis of Performance metric, Process variation, Underlapped FinFET and Temperature effect" IEEE Circuits and System Magazine, vol. 11, issue 2, pp. 38- 50, 2011.
- 5. Trew, R.J., High-frequency solid-state electronic devices. IEEE Transactions on Electron

Devices, 2005. 52(5): p. 638-649.

- S. Notomi, Y. Awano, M. Kosugi, T. Nagata, K. Kosemura, M. Ono, N. Kobayashi, H. Ishiwari, K. Odani, T. Mimura, and M. Abe, "A high-speed 1K4-bit static RAM using 0.5-m-gate HEMT," in Proc. GaAs IC Symp., 1987, pp. 177–180.
- B Raj, Quantum Mechanical Potential Modeling of FinFET, Toward Quantum FinFET, 81-97, 2013. (6)
- 8. VK Sharma, M Pattanaik, B Raj, PVT variations aware low leakage INDEP approach for nanoscale CMOS circuits, Microelectronics Reliability, Vol. 54, 90-99, 2014 9
- B. Raj, A. K. Saxena and S. Dasgupta, "Quantum Mechanical Analytical Modeling of Nanoscale DG FinFET: Evaluation of Potential, Threshold Voltage and Source/Drain Resistance "Elsevier's Journal of Material Science in Semiconductor Processing, Elsevier, Vol. 16, issue 4, pp. 1131- 1137, 2013. 6
- 10. VK Sharma, M Pattanaik, B Raj, INDEP approach for leakage reduction in nanoscale CMOS circuits, International Journal of Electronics 102 (2), 200-215 5
- 11. "ATLAS User Manual" by SILVACO Inc. January 23, 2013.
- 12. S Singh, B Raj,"Modeling and Simulation analysis of SiGe hetrojunction Double GateVertical t-shaped Tunnel FET", Superlattices and Microstructures, Elsevier Volume 142, PP. 106496, June 2020.
- S Singh, B Raj, "A 2-D Analytical Surface Potential and Drain current Modeling of Double-Gate Vertical t-shaped Tunnel FET", Journal of Computational Electronics, Springer, Vol. 19, PP.1154–1163, Apl 2020.
- S Singh, S Bala, B Raj, Br Raj," Improved Sensitivity of Dielectric Modulated Junctionless Transistor for Nanoscale Biosensor Design", Sensor Letter, ASP, Vol.18, PP.328–333, Apl 2020.
- 15. V Kumar, S Kumar and B Raj, "Design and Performance Analysis of ASIC for IoT Applications" Sensor Letter ASP, Vol. 18, PP. 31–38, Jan 2020.
- 16. G Wadhwa, B Raj, "Design and Performance Analysis of Junctionless TFET Biosensor for high sensitivity" IEEE Nanotechnology, Vol.18, PP. 567 574, 2019.
- 17. T Wadhera, D Kakkar, G Wadhwa, B Raj, "Recent Advances and Progress in Development of the Field Effect Transistor Biosensor: A Review" Journal of ELECTRONIC MATERIALS, Springer, Volume 48, <u>Issue 12</u>, pp 7635–7646, December 2019.
- 18. S Singh, B Raj, "Design and analysis of hetrojunction Vertical T-shaped Tunnel Field Effect Transistor", Journal of Electronics Material, Springer, Volume 48, <u>Issue 10</u>, pp 6253–6260, October 2019.
- 19. C Goyal, J S Ubhi and B Raj, "A Low Leakage CNTFET based Inexact Full Adder for Low Power Image Processing Applications", International Journal of Circuit Theory and Applications, Wiley, <u>Volume47, Issue9</u>, Pages 1446-1458, September 2019.
- Sharma, S. K., Raj, B., Khosla, M., "Enhanced Photosensivity of Highly Spectrum Selective Cylindrical Gate In1-xGaxAs Nanowire MOSFET Photodetector, Modern Physics letter-B, <u>Vol. 33, No. 12</u>, PP. <u>1950144 (2019)</u>.
- 21. J Singh, B Raj, "Design and Investigation of 7T2M NVSARM with Enhanced Stability and Temperature Impact on Store/Restore Energy", IEEE Transactions on Very Large Scale Integration Systems, Vol. 27, Issure 6, PP. 1322 1328 June 2019.
- 22. A K Bhardwaj, S Gupta, B Raj, Amandeep Singh, "Impact of Double Gate Geometry on the Performance of Carbon Nanotube Field Effect Transistor Structures for Low Power Digital Design", Computational and Theoretical Nanoscience, ASP, Vol. 16, PP. 1813–1820, 2019.
- C Goyal, J SUbhi and B Raj, Low Leakage Zero Ground Noise Nanoscale Full Adder using Source Biasing Technique, "Journal of Nanoelectronics and Optoelectronics", American Scientific Publishers, Vol. 14, PP. 360–370, March 2019.

- A Singh, M Khosla, B Raj, "Design and Analysis of Dynamically Configurable Electrostatic Doped Carbon Nanotube Tunnel FET"," Microelectronics Journal, Elesvier, <u>Volume 85</u>, Pages 17-24, March 2019.
- 25. C Goyal, J S Ubhi and B Raj, A reliable leakage reduction technique for approximate full adder with reduced ground bounce noise, Journal of Mathematical Problems in Engineering, Hindawi, Volume 2018, Article ID 3501041, 16 pages, 15 Oct 2018.
- 26. G Wadhwa, B Raj, "Label Free Detection of Biomolecules using Charge-Plasma-Based Gate Underlap Dielectric Modulated Junctionless TFET" Journal of Electronic Materials (JEMS), Springer, Volume 47, <u>Issue 8</u>, pp 4683–4693, August 2018
- 27. G Wadhwa, B Raj, "Parametric Variation Analysis of Charge-Plasma-based Dielectric Modulated JLTFET for Biosensor Application" IEEE Sensor Journal, VOL. 18, NO. 15, AUGUST 1, 2018
- 28. D Yadav, S S Chouhan, S K Vishvakarma and B Raj, " Application Specific Microcontroller Design for IoT based WSN", Sensor Letter, ASP, Vol. 16, PP. 374–385, May 2018