Drain Current Analysis with Process Parameters Variations of Nanowire TFET

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Abstract

This paper presents the drain current analyses for the different parameters of Nanowire tunnel field-effect transistor (TFET). The device has been designed using an n-channel P^+-I-N^+ structure for tunneling junction of TFET with gate-all-around (GAA) Nanowire. The gate length has been taken as 100 nm using silicon Nanowire to obtain the various parameters such as ON-current (I_{ON}), OFF-current (I_{OFF}), current ratio, and Subthreshold slope (SS) by applying different values of work function at the gate, the radius of Nanowire and oxide thickness of the device. The simulations are performed on Silvaco TCAD which gives a better parametric analysis over conventional tunnel field-effect transistor. The results obtained will be useful for the scientific and research community working in this area.

Keywords

Drain Current (I_D), Gate All Around (GAA), Nanowire (NW), Gaussian doping (GD), TFET.

1. Introduction

The regular scaling in metal oxide semiconductor field effect transistors (MOSFETs) is very difficult due to various aspects such as current carrier mechanism (thermal emission of electrons); higher short channel effects (SCEs), high OFF current and limited subthreshold slope (60mV/decade) in the Nanoscale regimes [1]–[8]. The main demerit of MOSFET is Subthreshold Slope (SS) which is defined as rate of increase in output (drain) current with the increase in the gate-source voltage (V_{gs}) from 0 volt. The higher SS are effects the supply voltages, which is required for the switching of device from OFF state to ON state [9]–[12]. For the development of new devices in the semiconductor; there is need to be especially low power, lower SS and power efficient device. The tunnel field effect transistor (TFET) is most preferable candidate in the semiconductor industry from the last decade [13]–[18]. The current carrier mechanism of TFET is performed by tunneling instead of thermionic emission. The structure of TFET is in asymmetrical nature (p-i-n) with different material of source and drain (either n-type or p-type). TFET has number of merits which overcomes the problem of MOSFET such as low Subthreshold Slope (SS) which is suitable for low power supply, reduced SCEs [19]–[23] and low OFF-current (I_{OFF}) due to band to band tunneling mechanism; but it suffers from low ON-current (I_{ON}), which is required for high speed operation of the device. So it should be needed that an advance device which mitigates the problem of low I_{ON} and operating speed. The Nanowire based TFET structures have the potential to gives the better results in terms of high ON-current and higher operation speed with reduced SCEs [12], [24]–[26]. So we have designed and simulate gate all around Nanowire TFET (NWTFET) and analyze its various parameters such as I_{ON}, I_{OFF}, ON-OFF current

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ratio (I_{ON}/I_{OFF}) and SS with the impact of its dimensional parameters such as gate length, oxide thickness and radius of Nanowire.

2. Device Structure

The structure of designed gate all around Nanowire TFET (NWTFET) is shown in Figure 1. The basic p^+-i-n^+ structure of TFET is used for device designing with Silicon GAA Nanowire. The basic parameters NWTFET taken as gate length (L_g) = 100 nm, Nanowire Radius (R) = 10 nm, Source/Drain length ($L_{s/d}$) = 80 nm, thickness of gate oxide (T_{ox}) = 1.5 nm with Gaussian doping concentration are used for simulation of the device using Silvaco Atlas Tools.

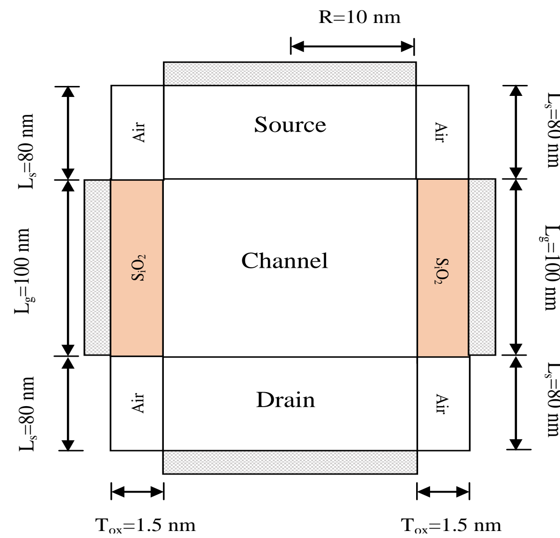

Figure 1: Strcture of NWTFET

The high source/drain doping concentration, channel doping concentration and gate-workfunction of NWTFET are taken as $1*10^{-19}$ cm^{-3}, $1*10^{-17}$ cm^{-3} and 4.3 eV respectively. The Silicon thickness are maintained under Debye-length; as$\sqrt{([(\epsilon_si\ V_T)/q +\ 60.N]\ )}$, where as q, N, V_T represents the charge of electron, concentration and thermal voltage respectively while ϵ_{si} refer as dielectric constant [27]. The proposed structure is calibrated with reported conventional TFET structure [19]. The basic parameters of conventional device are taken same as reported in ref [19]. The calibration has been done using plot digitizer tools and Silvaco Simulation Tool. The calibration curve of NWTFET is shown in Figure 2.

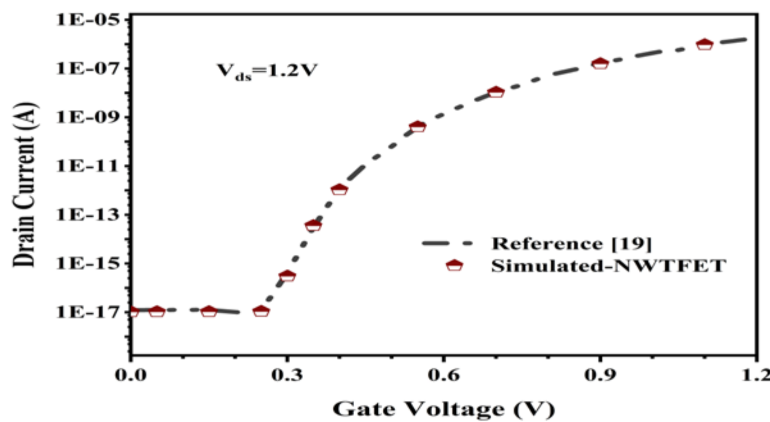

Figure 2: Calibration Curve of NWTFET with ref [19]

The different models have been used for simulations such as BTBT model for tunneling, BGN model for the effect of bandgap and FLDMOB for field-dependent mobility as well as FERMI model for Fermi–Dirac statistics with the addition of CVT model. The used parameter for NWTFET designing is illustrating in Table 1.

Table 1
Parameter of NWTFET

Parameters	Values
Gate length (L_g)	100 nm
Work-function of Gate (ϕ_g)	4.3eV
Thickness of gate oxide (T_{ox})	2.5 nm
Nanowire Radius (R)	20 nm
Channel Concentration	1×10^{17}cm^{-3}
Source/Drain Concentration	1×10^{19}cm^{-3}

Figure 3. Illustrate the energy band diagrams of NWTFET in ON state and OFF state which is performing as tunneling actions during simulation process. When the gate voltage is equal to zero and greater than zero (~1.5V), device will act as OFF state (dash line) and ON state (solid line) respectively by applying drain-source voltage is 1.0 V as shown in Figure 3. The energy gap between valance band and conduction band is higher in OFF state but lesser in ON state. So the tunneling of electrons has possible only in ON state as shown in energy band diagram.

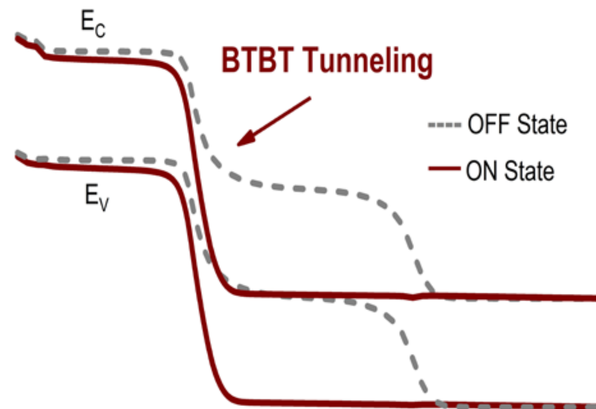

Figure 3: Energy band diagram of NWTFET

3. Result and Simulation

The result and simulation of NWTFET are explained in this section by using Silvaco simulation tool. To calculate the different parameters such as drain current, ON/OFF ratio and SS, dimensional parameters has been varied such as gate work-function (ϕ_g), oxide thickness and radius of Nanowire. The drain current variation of NEFET are observed with the effect/impact of different parameters such as

3.1 Effect of work-function (ϕ_g)

Firstly, the I_D characteristics are observed with different ϕ_g and taken as 4.0 eV and 4.3 eV shown in Figure 4. For the simulation work the gate voltage varied from -0.2 to 1.2 voltage and drain-source voltage (V_{ds}) taken as 1.2V. According to Figure 4, the maximum ON current (3.60×10^{-6}) and minimum SS (20.25 mV/dec) are observed at ϕ_g =4.0 eV, but OFF (2.45×10^{-13}) current is also high

which leads the SCEs. On the other hand lower OFF current is observed at 4.3 eV. So ϕ_g =4.3 has been taken for proposed device for minimum SCEs.

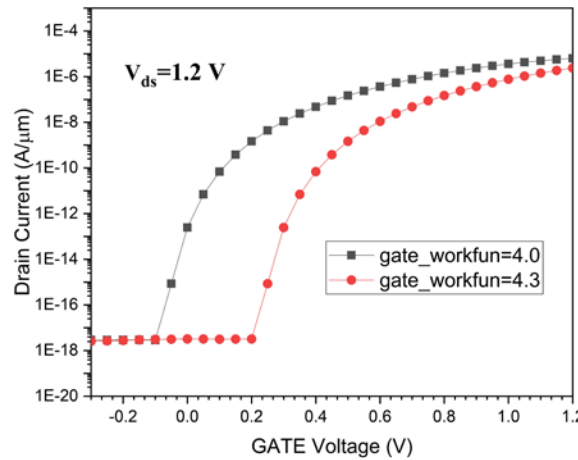

Figure 4: Effect of gate work-function on drain current

3.2 Effect of oxide thickness (T_{ox})

Secondly, the I_D characteristics are observed with different T_{ox} (1.5 nm and 3.5 nm). Figure 5 illustrates the simulation work of NWTFET on drain current with the impact of different T_{ox} at 1.2V drain-source voltage. It is observed that better parametric value of I_D and current ratio with minimum SS (19.40) at Tox=1.5 nm. During the simulation process ϕ_g , R and T_{ox} has been taken as 4.3 eV, 20 nm and 3.5 nm respectively. The minimum value oxide thickness has given good parametric values and lesser leakage current in the device.

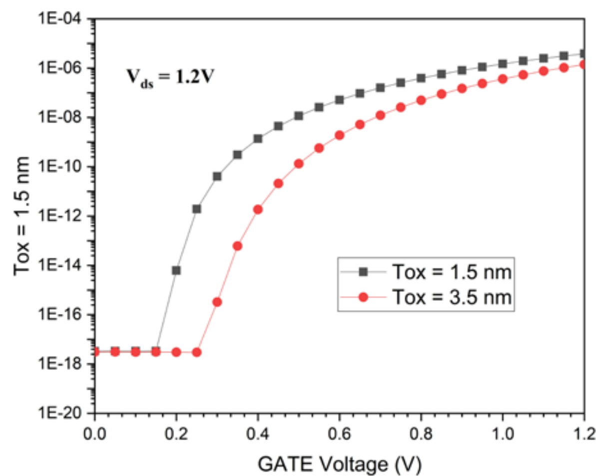

Figure 5: Drain current variation due to effect of T_{ox}

3.3 Effect of Nanowire Radius (R)

The drain current variation with the effect of nanowire radiu are shown in Figur 6. According to characteristics curve it observed that higher I_{ON} (7.63×10^{-7}) at R= 20 nm, but the I_{OFF} current is also higher at this stage. Due to R variation on NWTFET the better SS (15. 22) has been archived on 10 nm. During to simulation work, gate voltage is varied from 0 to 1.5 and V_{ds}=1.2.

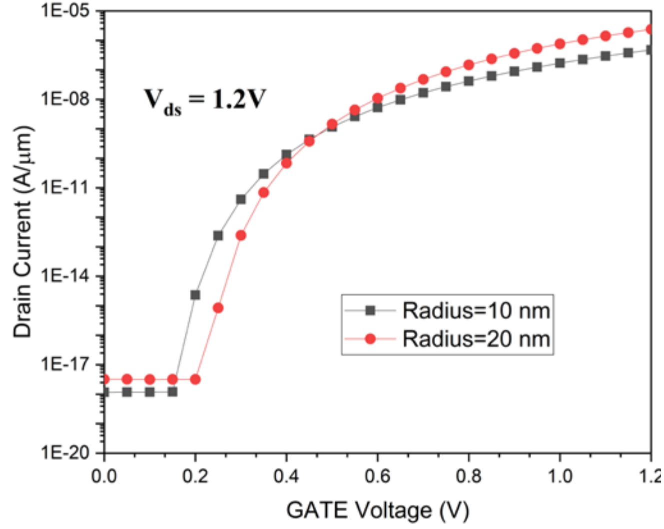

Figure 5: Drain current variation due to effect of Radius (R)

The detailed observed parametric values are given in Table 2.

Table 2
Parameters of NWTFET after Simulation

Parameter	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/ I_{OFF} Ratio	SS (mV/dec)
ϕ_g = 4.0 eV	3.60×10^{-6}	2.45×10^{-13}	1.47×10^{7}	20.25
ϕ_g = 4.3 eV	7.63×10^{-7}	3.23×10^{-18}	2.36×10^{11}	20.32
T_{ox} = 1.5 nm	2.05×10^{-6}	2.95×10^{-19}	6.94×10^{12}	19.40
T_{ox} = 3.5 nm	1.71×10^{-6}	7.40×10^{-19}	2.31×10^{12}	25.67
R = 10 nm	1.69×10^{-7}	1.17×10^{-18}	1.45×10^{11}	15.22
R = 20 nm	7.63×10^{-7}	3.23×10^{-18}	2.36×10^{11}	20.32

4. Conclusion

The device NWTFET has been designed and simulated using Gaussian doping profile and analyzed parametric variations of I_{ON}, I_{OFF}, I_{ON}/I_{OFF} and SS. The simulated results have also shows the effect on drain-current (I_d) with impact of Tox, R and ϕ_g of the device. The most suitable parametric value are observed such as I_{ON} = 3.60x10^{-6} A/μm, I_{OFF} = 2.95x10^{-19} A/μm, SS = 15.22 mV/dec and $I_{ON/OFF}$ = 6.94×10^{12}. The proposed NWTFET device structure will be suitable for low power applications.

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